Code: 211.071.101
Date: April 9, 1956

IBM

TECHNICAL REPORT

ELECTRONIC AUTOMATIC ADDRESSING

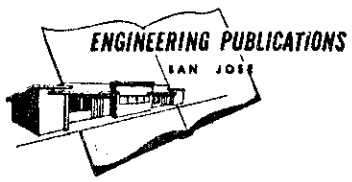
BY

F. B. WOOD

IBM ADVANCED DEVELOPMENT LABORATORY
San Jose, California

ABSTRACT

This is the concluding report as of August 1955, on a proposal for an electronic system of automatic addressing for RAMAC. This proposal was developed at a time when the available programmed addressing system used a large fraction of the file space. This system was proposed as an optional addition to a RAMAC having one-hundred heads ganged on one access mechanism. Five extra tracks per disk side are added to carry the addressing index. The external address or catalog numbers are written in parallel, one bit per head in these addressing tracks. The internal address is counted by a clock register as the address tracks are scanned in parallel for coincidence with the desired catalog number.



INTERNATIONAL BUSINESS MACHINES CORPORATION
SAN JOSE, CALIFORNIA

A PROPOSAL FOR ELECTRONIC AUTOMATIC ADDRESSING

Introduction

This is a concluding report on a proposal for an electronic system of automatic addressing for RAMAC. This proposal was developed at a time when the available programmed addressing system used a large fraction of the file space for indexing. For an early example of programmed addressing refer to the preliminary 305 manual.[1] This programmed system uses 21 disks out of the 50 for indexing 25,000 items. Other programmed automatic addressing systems were developed by the Product Planning Division for particular applications such that a smaller fraction of the file was required for indexing. Other systems of programmed addressing were proposed by M. L. Lesser which reduced the fraction of the file required for indexing by addition of an electronic high-equal-low comparator to the RAMAC processing circuits.

As work proceded on this proposal, advances[2] were made in the analysis of the addressing problem and improved programmed addressing systems were developed. One system developed by J. J. Nolan[3] uses a minimum of processing time and file space, such that it is not economically feasible to do any further development work on the electronic automatic addressing system of this proposal.

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1 "IBM Random Access Accounting Machine Type 305: Manual of Operation" Preliminary Edition (From 22-6264-0), pp. 47-48.

2 Peterson and Haibt, "Proceedings of the Conference on Index Numbers and methods", IBM TR 001.0110575, June 1955.

3 J. J. Nolan, "Programmed Address Conversion for the IBM 305 RAMAC" Product Planning Division, San Jose Laboratory, RAMAC Bulletin No. 1, November 15, 1955.

DESCRIPTION OF THE SYSTEM

One of the proposed systems of electronic automatic addressing is shown in Figures 1 - 4. This system uses a minimum of operations involving the RAMAC processing drum so the addressing operation can be overlapped with other processing. In this system the NRZI recording system for records is retained. For the address track recording in parallel the levels of magnetization are "plus", "blank", and "minus".

This system consists of 50 disks with 100 heads on one access arm. This reduces the access time from (200 - 600 ms) to (60 - 110ms) by eliminating the physical moving of the access arm from disk to disk. The system is illustrated by the following block diagrams:

Figure 1 - RAMAC less Disk File
Figure 2 - Disk File, Heads, Fast Access and Switching Circuits
Figure 3 - Automatic Addressing: Coincidence, Blank Detection and Writing
Figure 4 - Automatic Addressing: Clock, Register, Address Buffer and Control Circuits

The following additions are required to the RAMAC access logic circuits:

$T_2 = W$ Set up relays AA for External Address
$Q = A$ Switch to Automatic Addressing Cycle

The sample instructions in the following descriptions are for a sixteen character alphanumeric external address placed in field 6 - 21 on the punched cards.

The relay positions are coded as follows:

0 - Access mechanism set to main record under control of process drum.
1 - Scanning of address tracks for coincidence parallel operations
2 - Scanning of address tracks for first blank
3 - Recording of External Address in Address Tracks
4 - Writing revised record into main file.
- Erasing uses 3 with reversed external address

The addressing tracks consist of five extra tracks outside of the regular 100 tracks on each disk side. Gliding magnetic heads for vertical magnetization are proposed. The present NRZI recording system and bit density of 57 to 101 bits per inch in the 100 record tracks would be continued. In the five addressing tracks the bit density would be increased to 160 bits per inch, (240 kc) in order to get 10,000 addresses in five tracks. Each external address would consist of 100 bits in parallel, one bit on each disk side. The internal address is the number of bit spaces from the start of the address tracks to the point where the external address is recorded.

Sequence of Operations

Step No.	Program Instruction	Description
00	S99A9900-A	Card input to track A on process Drum. Q=A Switches relays from stage "O" to Stage 1. This sends RESET signal on Line 1 to set relays AZ, BA. This signal also resets: Thyratron AT Internal address register AI Internal address buffer AR Register subtract unit AK
01	A21W9916	Puts external address into relays AA by way of thyratron AT
(Processing drum available for other processing at this point)		The addressing track relay BA is wired so that on position 1, 2, and 3, the 80 and 20 cams move, putting the heads on track 100 (first addressing track) when gap register BI is on zero. The external address clock signal on Line 12 is fed through gate BL which is opened when "address on track" signal is followed by signal from gap detector.

Scanning

(1) For Coincidence

(These two operations are run in parallel. they would have to be run in series).

External address clock pulses through Gate BL and AQ operate internal address buffer AR while the output of the 100 heads RB is run through the 100 relays AA set up for the external address through preamplifier AC to both:

- External Address Coincidence OR Circuit AO and

When coincidence is found the output from AO closes gate AQ through OR circuit AP, stopping buffer AR, which then reads internal address corresponding to the specified external address. It also through gate AV and delay AW reads out internal address buffer AR to the RAMAC process address buffer.

(2) For First Blank

For a two-level magnetization system

External address clock pulses through gates BL operate internal address clock register AI while the output of three heads are examined for blanks by OR circuit AD.

both:

- Blank Detection OR Circuit AD

When a blank is found a signal goes to trigger and gate AF, which inhibits gate AG, stopping internal address clock register AI, and closing gate AF. Blank found signal and buffer overflow signals trigger the register subtract circuit AK through and circuit AJ.
Register subtract circuit AK resets gap register BI through trigger and gate AI. This resets track selector to track 100. Then internal address clock register reads backward.

(3) Writing External Address

When it goes through zero the zero detects BJ triggers external address write amplifier AM. This zero detector signal also closes gate AQ through AP, stopping internal address buffer AR on site of blank to be filled, and also sets gate AV which through delay BK switches RAMAC to processing after reading out internal address..

Both steps (1) and the step (2) and (3) leave the internal address set up in the processing address buffer.

Step No.	Program Instruction	Description
02	R99B99002 (Program steps)	Seek record, bring to track B. Ends with revised record in track A.
03	A99R9900	Write revised record in file.

Erasing of Obsolete Records

Erasing of obsolete records can be taken care of by including the following program steps in the program:

Step No.	Program Instruction	Description
10	T00A8001BC	Compare column 80 of card for blank. If card is to be deleted P=B signal reverses switch at External Address Amplifier AM and switches in Step (3) after Step (1). This cancels out external address in address track.
11	---R9900--	Erases record at internal address left set up in processing address buffer.

The logic is such that P=B also sends out a reset 1 signal so that the internal address is stored in the clock register AI in addition to reading out into processing address buffer.

Time of Addressing Operation

A set of maximum and minimum time schedules for automatic addressing are shown in Figure 5. The time to find the internal address and to bring the record to the processing drum varies from 460 to 830 milliseconds depending upon how much of the address section must be scanned to find it. The longer time for entering new records is due to scanning the entire address record to verify that it is not already in the file. To shorten the initial loading a control panel switch could be provided to cut out the coincidence scanning temporarily to save time.

Cost Estimate for Automatic Addressing

Although no plate model has been built the approximate cost can be estimated from the number of relays, tubes, transistors, and heads required for the logical circuits shown in Figure 1 through 4. The following cost estimate is based on first changing the RAMAC to faster access by having one head per disk side.

Fast Access	Savings by Deletion of RAMAC Component Omitted		Cost of New Components	
Access Mechanism		$925		
Air Compressor		100		
Track Access Cams				$525
Track Access Bail, Combs and Detents				
Air Head	$25 x 2 =	50		
Gliding Magnetic Heads			$4 x 100 =	400
Null Detector and Servo Amp.		75		
Track Address		50	$5 x 15 =	75
Markite Relay Networks		100		
Disk and Side Access Networks			$5 x 20 =	100
Floating Power Supply		25		
Aluminum Disk				
Steel Disks for Vertical Recording		--		--
		$1325		$1100
	Net Savings	$ 225		

Automatic Addressing — Cost of New Components

	50 - bit		100 - bit	
Changes in Logic Circuits		30	$5 x 6dt =	30
External Address Relays AA	$5 x 50 =	250	$5 x 100 =	500
Pre-Amps (Transistors) AC	$2 x 200 =	400	$2 x 400 =	800
Switching Relays A2-BC	$5 x 38 =	190	$5 x 50 =	250
		20	$5 x 4dt =	20
		4	$2 x 2dd =	4
Thyratron AT	$5 x 50 =	250	$5 x 100	500
External Address Coincidence Or, AO	$5 x 50 =	250	$5 x 100vd	500
Clock Register AI		100	$5 x 20	100
Internal Address Buffer AR		100	$5 x 20	100
Other Gates, Detection, Amplifier				
Double Diodes		42	$2 x 21	42
Double Triodes		105	$5 x 21	105
		$1741		$2951
Less Fast Access Saving		225		225
		$1510		$2726
Further Savings in Pre-Amplifiers if Ferranti Phase Modulation System of Recording is Used		200		400
		$1316		$2326

Acknowledgements

The basic system of recording external addresses with the bits in parallel in the address tracks as used in this proposal was originally proposed by L. D. Stevens. The general plan for the automatic addressing logic was developed by J. J. Hagopian and F. B. Wood. The vertical magnetic heads were designed by J. J. Hagopian and were tested by W. A. Holman. The mechanical binary cam and detent system for locating the heads on the tracks was designed by R. V. Muffley. J. W. Beck designed the track selector relay networks, interlocks, and the tentative transistor pre-amplifiers. F. B. Wood designed the disk selector networks.

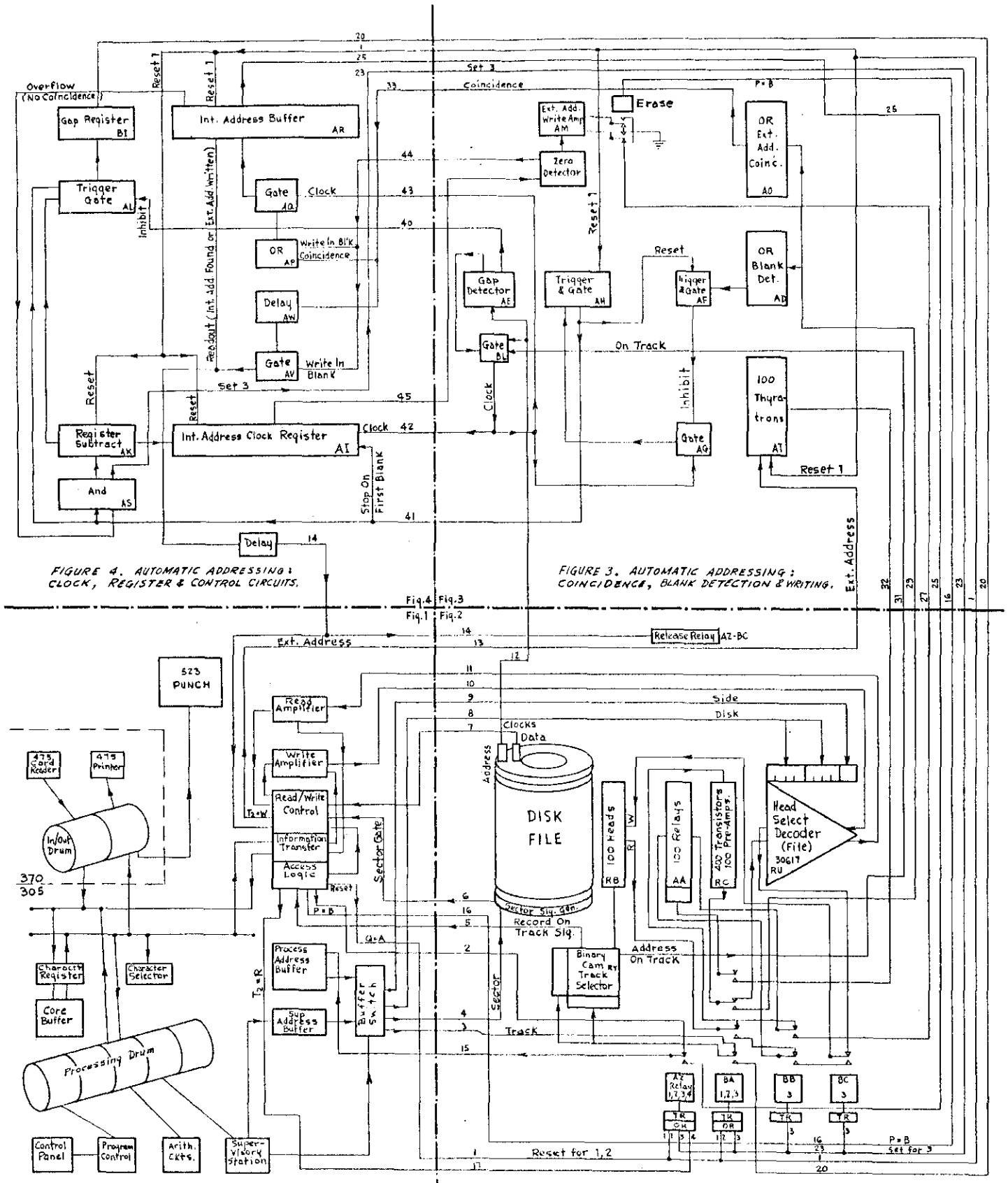

FIGURE 4. AUTOMATIC ADDRESSING: CLOCK, REGISTER & CONTROL CIRCUITS.

FIGURE 3. AUTOMATIC ADDRESSING: COINCIDENCE, BLANK DETECTION & WRITING.

Fig.4 Fig.3
Fig.1 Fig.2

FIGURE 1. RAMAC LESS DISK FILE.

FIGURE 2. DISK FILE, HEADS, FAST ACCESS & SWITCHING CIRCUITS.

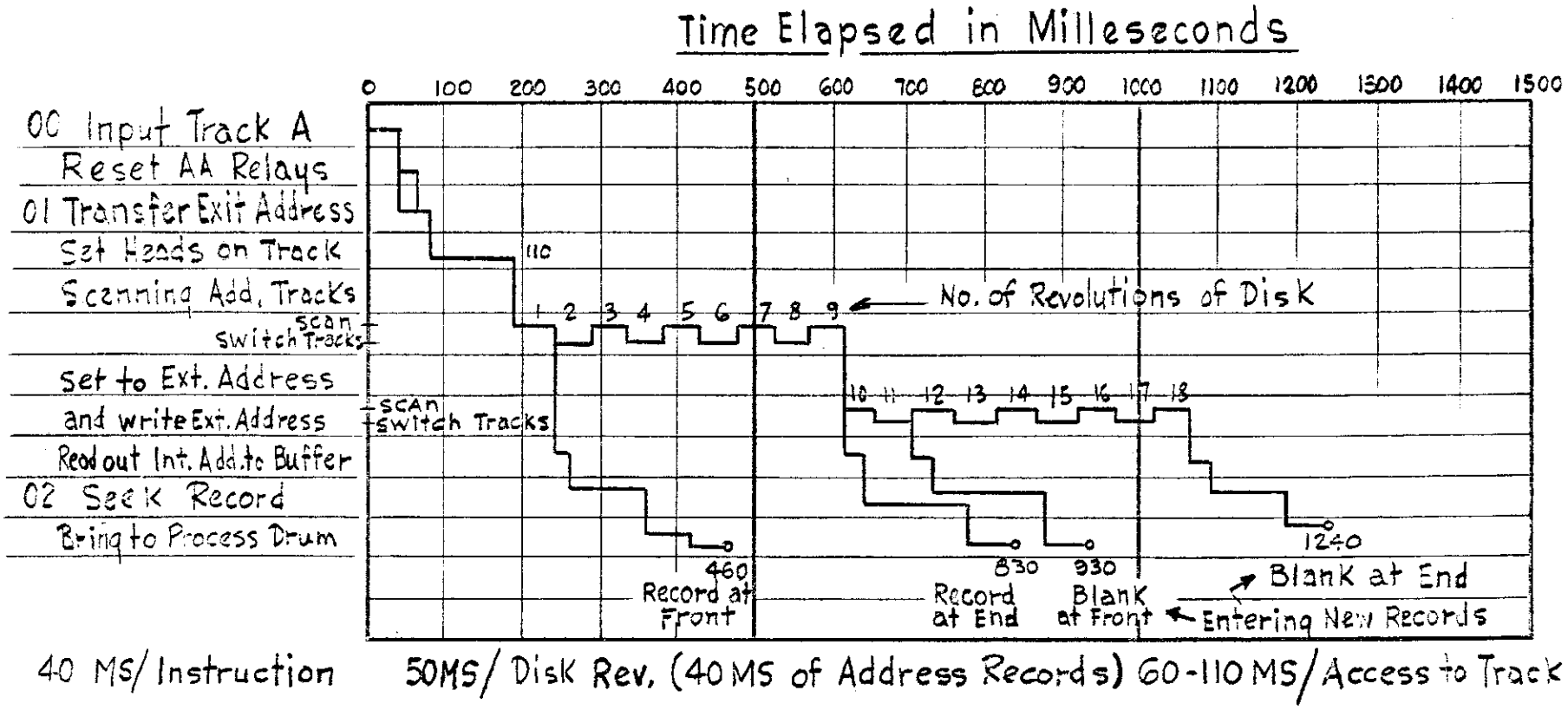

FIGURE 5.- TIMING SCHEDULE for AUTOMATIC ADDRESSING